


Substitute for Form 1449A/PTO (Modified)		Attorney Docket No.: 42390.P8533	Application Number: 09/608,856
Sheet 1 of 4		First Named Inventor: Jin Yang	Examiner: Unassigned
		Filing Date: June 30, 2000	Art Unit: 2123

U.S. PATENT DOCUMENTS

Exam. Initial*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Document	Date of Publication of Cited Document MM-DD-YYYY	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (If known)			
AB		5,469,367		Puri et al	11-21-1995	
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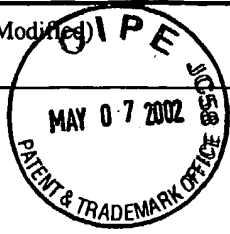
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¹Unique citation designation number. ²See attached Kinds of U.S. Patent Documents. ³Enter Office that issued the document, by the two-letter code (WIPO Standard S.3). ⁴For Japanese patent documents, the indication of the year of reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

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Substitute for Form 1449A/PTO (Modified) (use as many sheets as necessary)	Attorney Docket No.: 42390.P8533	Application Number: 09/608,856
Sheet 2 of 4	First Named Inventor: Jin Yang	Examiner: Unassigned
	Filing Date: June 30, 2000	Art Unit: 2123



OTHER ART - NO PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
MB		BEREZIN, S. et al, "A Compositional Proof System for the Modal μ -Calculus and CCS," <i>Technical Report CMU-CS-97-105, Carnegie Mellon University, January 15, 1997</i>	
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		CHEN, Y. et al, "PBHD: An Efficient Graph Representation for Floating Point Circuit Verification," <i>Technical Report CMU-CS-97-134, Carnegie Mellon University, May 1997</i>	
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Sheet 3 of 4		First Named Inventor: Jin Yang	Examiner: Unassigned
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Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
AB		CHOU, C., "The Mathematical Foundation of Symbolic Trajectory Evaluation," <i>International Conference on Computer-Aided Verification(CAV'99)</i> , Trento, Italy, July 1999 pp. 196-207, Proceedings of CAV'99, Lecture Notes in Computer Science #1633 (Editors: Nicolas Halbwachs & Doron Peled), Springer-Verlog, 1999	
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✓		JAIN, A. et al, "Verifying Nondeterministic Implementations of Determinist Systems," <i>Lecture Notes in Computer Science, Formal Methods in Computer Aided-Design</i> , pp. 109-125, November 1996	

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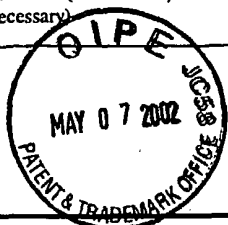
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Sheet 4 of 4	First Named Inventor: Jin Yang	Examiner: Unassigned
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AS		JAIN, A., "Formal Hardware Verification by Symbolic Trajectory Evaluation," <i>Carnegie Mellon University Ph.D. Dissertation</i> , July 1997	
		JAIN, S. et al, "Automatic Clock Abstraction from Sequential Circuits," <i>Proceedings of the 32nd ACM/IEEE Conference on Design Automation</i> , January 1995	
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		YEH, W. et al, "Compositional Reachability Analysis Using Process Algebra," <i>28th ACM/IEEE Design Automation Conference</i> , 1991	
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Sheet 1 of 1		First Named Inventor: Jin Yang	Examiner: Unassigned
		Filing Date: June 30, 2000	Art Unit: 2123
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Examiner Initials*	Cite No ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published	Translation ²
AB		BRADLEY, J., et al., "Compositional BDD Construction: A Lazy Algorithm," Department of Computer Science, University of Bristol, UK, April 6, 1998	
↓		BURCH, E. M., et al., "Symbolic Model Checking for Sequential Circuit Verification," <u>IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems</u> , Volume 13, Issue 4, April 1994, pp. 401-424	
		CAMPOS, S.V.A., "Symbolic Model Checking in Practice," <u>XII Symposium on Integrated Circuits and Systems Design, 1999 Natal, Brazil - IEEE</u> , September 1999, pp. 98-101	
		HOJATI, R., et al., "Early Quantification and Partitioned Transition Relations," <u>1999 IEEE International Conference on Computer Design: VLSI in Computers and Processors, 1996, ICCD '96 Proceedings - Austin, TX, October, 1996</u> , pp. 12-19	
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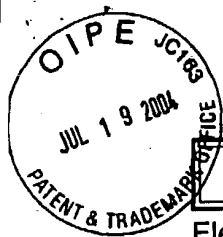
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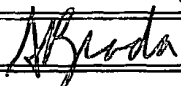
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Title of Invention	Methods for performing generalized trajectory evaluation						
Application Number: 09/608856							
Confirmation Number: 2493							
First Named Applicant: Jin Yang							
Attorney Docket Number: 42P8533							
Art Unit: 2123							
Examiner: Samuel Broda							
Search string: (5870590 or 6484134).pn.							
US Patent Documents							
Note: Applicant is not required to submit a paper copy of cited US Patent Documents							
init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
	1	5870590	1999-02-09	Kita et al.			
	2	6484134	2002-11-19	Hoskote			
Signature							
Examiner Name				Date			
				9/18/04			